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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,486	PULLEN ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
- after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 July 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/8/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 7/8/2003 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: In each Figure there are many items that are not mentioned in the Specifications. A few examples are from Figure 1A with items 104, 105, 115, 117, 124, 126 140 and 180. Similar situations occur in Figures 2, 3, 4A, 4B, 5 and 6. Also in Figure 1A items 101 and 102 should be switched as well as 142 should be 141(per Specifications). Also, in Figure 1B VR5 should be VR2. There are also items mentioned in the Specifications that do not appear in the drawings such as items 500, 518, 118, 229, 252, 200, 329, 352, 305(maybe should be 306), and 337. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top

margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith(US Patent 5,309.344).

As to claim 1, Smith discloses a multiphase buck converter system with peak current sharing comprising a first buck converter(first converter 100, see Fig. 8) coupled to a first regulator input voltage(input supply 801, see Fig. 8) and generating a first converter output voltage(output 802, see Fig. 8) for powering a common load(load 174, see Fig. 4) in response to a first ON-time(ON-period, see column 6, line 39) pulse set to a first logic state by a first start signal(first duty cycle signal S1, see Fig. 8) and set to a second logic state by a first stop signal(first control bus 805, see Fig. 8), wherein the first converter output voltage supplies energy to the common load directly from the first regulator input voltage when the first ON-time pulse has the first logic state and the first converter output voltage supplies stored energy from the first regulator input voltage

when the first ON-time pulse has the second logic state. Smith also discloses a second buck converter(second converter 100', see Fig. 8) coupled to a second regulator input voltage(input supply 801, see Fig. 8) and generating a second converter output voltage(output 802, see Fig. 8) for powering the common load in response to a second ON-time pulse set to a first logic state by a second start signal(second duty cycle signal S2, see Fig. 8) and set to a second logic state by a second stop signal(second control bus 806, see Fig. 8), wherein the second converter output voltage supplies energy to the common load directly from the second regulator input voltage when the second ON-time pulse has the first logic state and the second converter output voltage supplies stored energy from the second regulator input voltage when the second ON-time pulse has the second logic state. Further Smith discloses a start circuitry(PWM means 910, see Fig. 8) for generating the first and second start signals in response to a regulated voltage across the common load, a reference voltage(Vcc, see Fig. 8), and the first and second ON-time pulses, a first stop circuitry(first control means 970, see Fig. 8) for generating the first stop signal in response to the first regulator input voltage and the reference voltage, and a second stop circuitry(second control means 999, see Fig. 8) for generating the second stop signal in response to a first output current(I sub s, see Fig. 11A) from the first converter output voltage supplied to the common load, a second output current(I sub s, see Fig. 11A) from the second converter output voltage supplied to the common load, and the first ON-time pulse.

As to claim 2, Smith discloses the converter system wherein the first stop circuitry comprises a capacitor(capacitor 956, see Fig. 11A) charged by a current from

the first regulator input voltage when the first ON-time pulse has the first logic state and discharged when the first ON- time pulse has the second logic state, and first compare circuitry(controller 90, see Fig. 11A) for comparing the reference voltage to a capacitor voltage across the capacitor and generating the first stop signal, wherein the first stop signal has a first logic state when the capacitor voltage is greater than the reference voltage and a second logic state when the capacitor voltage is less than the reference voltage.

As to claim 3, Smith discloses the converter system wherein the second stop circuitry comprises peak circuitry for generating a peak voltage(output voltage of the error amplifier, see column 49, line 22) proportional to a peak value(threshold level, see column 49, line 43) of the first output current, first sense circuitry for generating a first sense voltage(V sub FB, see Fig. 11A) proportional to the second output current, and second compare circuitry(controller 960, see Fig. 11A) for comparing the first sense voltage to the peak voltage and generating the second stop signal, wherein the second stop signal has a first logic state when the first sense voltage is greater than the peak voltage and a second logic state when the first sense voltage is less than the peak voltage.

As to claim 4, Smith discloses the converter system wherein the first sense circuitry comprises a first sense resistor(resistors 941 and 942, see Fig. 11A) having a first terminal coupled to the first converter output voltage and a second terminal coupled to the common load, and a differential amplifier(error amplifier, see column 48, line 39) having a positive input coupled to the first terminal of the first sense resistor and a

negative input coupled to the second terminal of the first sense resistor, and an output generating the first sense voltage.

As to claim 5, Smith discloses the converter system wherein the peak circuitry comprises a second sense resistor(resistors 941 and 942, see Fig. 11A) having a first terminal coupled to the second converter output voltage and a second terminal coupled to the common load, a differential amplifier(error amplifier, see column 48, line 39) having a positive input coupled to the first terminal of the second sense resistor and a negative input coupled to the second terminal of the second sense resistor, and an output generating the second sense voltage, and a sampling circuit(flip-flop 930, see Fig. 11A) for tracking the second sense voltage when the first ON- time pulse has the first logic state and holding a value of the second sense voltage as the peak voltage when the ON-time pulse has the second logic state.

As to claim 6, Smith discloses the converter system wherein the start circuitry comprises a compare circuit(controllers 950 and 960, see Fig. 11A) for comparing the regulated voltage across the common load to the reference voltage and generating a gate signal having a first logic state when the reference voltage is greater than the regulated voltage and a second logic state when the reference voltage is less than the regulated voltage. Smith also discloses a first select circuit(controller 950, see Fig. 11A) for generating the first start signal in response to the first ON-time pulse, the gate signal, the second start signal, and an initialization signal, and a second select circuit(controller 960, see Fig. 11A) for generating the second start signal in response to the second ON-time pulse, the gate signal, the first start signal, and the initialization signal.

As to claim 7, Smith discloses the converter system wherein the sampling circuit comprises a capacitor(capacitors 979 and 989, see Fig. 11B) having a first terminal coupled to ground and a second terminal, and an electronic switch(first control means 970, see Fig. 11B) for coupling the second sense voltage to the first terminal of the capacitor when the first ON-time pulse has the first logic state, the capacitor holding the value of the sense voltage as the peak voltage when the first ON-time pulse has the second logic state.

As to claim 8, Smith discloses the converter system wherein the first select circuit comprises a compare logic circuit(controllers 950 and 960, see Fig. 11A) for generating a compare logic signal in response to the regulated voltage across the common load, the reference voltage, and the initialization signal, and an initialization pulse(R/C clock, see Fig. 11A) circuit for generating an initialization pulse in response to the initialization signal and the compare logic signal. Smith also discloses a first logic circuit(controller 950, see Fig. 11A) for generating the first start signal in response to the first ON-time pulse, the initialization pulse, and the second start signal, and a second logic circuit(controller 960, see Fig. 11A) for generating the second start signal in response to the second ON-time pulse, the initialization pulse, and the first start signal.

As to claim 9, Smith discloses the converter system wherein the compare logic circuit comprises a comparator(controllers 950 and 960, see Fig. 11A) for comparing the reference voltage to the regulated voltage across the common load and generating a compare output signal having a first logic state when the reference voltage is greater than the regulated voltage across the common load and a second logic state when the

regulated voltage across the common load is greater than the reference voltage, and a logic gate(controllers 950 and 960, see Fig. 11A) generating the compare logic signal as logic combination of the compare output signal and the initialization signal.

As to claim 10, Smith discloses the converter system wherein the initialization pulse circuit comprises a logic gate(rectifier 988, see Fig. 11B) generating a start converter signal as a logic combination of the initialization signal and the compare logic signal, and a pulse circuit(second control means 999, see Fig. 11B) generating the initialization pulse in response to a logic transition of the start converter signal.

As to claim 11, Smith discloses the converter system wherein the first logic circuit comprises a flip-flop(flip-flop 930, see Fig. 11A) having an output(Q), an inverted output(Q/), a data input(D), a set input(D), a reset input(D), and a clock input(CK), wherein the set input is coupled to the initialization pulse, the clock input is coupled to the second start signal, and the inverted output is coupled to the data input, and a positive pulse circuit(second control means 999, see Fig. 11B) having an input coupled to the first start signal and an output coupled to the reset input of the flip-flop and generating a reset pulse in response to a logic transition of the first start signal. Smith also discloses an inverted pulse circuit(inverted buffer amplifier 982, see Fig. 11B) having an input coupled to the first ON-time pulse and an output generating an inverted pulse, wherein the inverted pulse circuit generates the inverted pulse in response to a logic transition of the first ON-time pulse. Smith further discloses a third logic circuit(rectifier 988, see Fig. 11B) having a first input coupled to the compare logic signal, a second input, a third input coupled to the output of the inverted pulse circuit,

and generating the first start signal, and a delay circuit(dual clock generator 920, see Fig. 11A) having an input coupled to the output of the flip-flop and a delay output coupled to the second input of the third logic circuit, wherein the delay circuit selectively delays a logic transition of the delay output.

As to claim 12, Smith discloses the converter system wherein the second logic circuit comprises a positive pulse circuit(second control means 999, see Fig. 11B) having an input coupled to the second start signal and an output generating a reset pulse on a logic transition of the second start signal, and a logic gate(rectifier 933, see Fig. 11A) having a first input coupled to the initialization pulse, a second input coupled to the output of the positive pulse circuit, and an output generating a gated reset pulse as a logic combination of the initialization pulse and the output of the positive pulse circuit. Smith also discloses a flip-flop(flip-flop 930, see Fig. 11A) having an output(Q), an inverted output(Q/), a data input(D), a reset input(D), and a clock input(CK), wherein the reset input is coupled to the output of the logic gate, the clock input is coupled to the first start signal, and the inverted output is coupled to the data input, and an inverted pulse circuit(inverted buffer amplifier 982, see Fig. 11B) having an input coupled to the first ON-time pulse and an output generating an inverted pulse, wherein the inverted pulse circuit generates the inverted pulse in response to a logic transition of the first ON-time pulse. Smith further discloses a third logic circuit(rectifier 988, see Fig. 11B) having a first input coupled to the compare logic signal, a second input, a third input coupled to the output of the inverted pulse circuit, and generating the second start signal, and a delay circuit(dual clock generator 920, see Fig. 11A) having an input

coupled to the output of the flip-flop and a delay output coupled to the second input of the third logic circuit, wherein the delay circuit delays a logic transition of the delay output.

As to claim 13, Smith discloses the converter system wherein the differential amplifier is a transconductance amplifier for converting a voltage across the first sense resistor to a first sense current coupled to a first resistor thereby generating the first sense voltage across the first resistor(see column 48, lines 36-60).

As to claim 14, Smith discloses the converter system wherein the differential amplifier is a transconductance amplifier for converting a voltage across the second sense resistor to a second sense current coupled to a second resistor thereby generating the second sense voltage across the second resistor(see column 48, lines 36-60).

As to claim 15, Smith discloses the converter system wherein the first ON-time pulse is generated as an output of a latch set by a first logic state of the first start signal and reset by a first logic state of the first stop signal(see Fig. 11A and 11B).

As to claim 16, Smith discloses the converter system wherein the second ON-time pulse is generated as an output of a latch set by a first logic state of the second start signal and reset by a first logic state of the second stop signal(see Fig. 11A and 11B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 17-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith(US Patent 5,309,344) in view of Nakagawa(US Patent 6,429,628).

As to claim 17, Smith discloses a system comprising a first buck converter(first converter 100, see Fig. 8) coupled to a first regulator input voltage(input supply 801, see Fig. 8) and generating a first converter output voltage(output 802, see Fig. 8) for powering a common load(load 174, see Fig. 4) in response to a first ON-time(ON-period, see column 6, line 39) pulse set to a first logic state by a first start signal(S1, see Fig. 8) and set to a second logic state by a first stop signal(first control bus 805, see Fig. 8), wherein the first converter output voltage supplies energy to the common load directly from the first regulator input voltage when the first ON-time pulse has the first logic state and the first converter output voltage supplies stored energy from the first

regulator input voltage when the first ON-time pulse has the second logic state. Smith also discloses a second buck converter(second converter 100', see Fig. 8) coupled to a second regulator input voltage(input supply 801, see Fig. 8) and generating a second converter output voltage(output 802, see Fig. 8) for powering the common load in response to a second ON-time pulse set to a first logic state by a second start signal(S2, see Fig. 8) and set to a second logic state by a second stop signal(second control bus 806, see Fig. 8), wherein the second converter output voltage supplies energy to the common load directly from the second regulator input voltage when the second ON-time pulse has the first logic state and the second converter output voltage supplies stored energy from the second regulator input voltage when the second ON-time pulse has the second logic state, and a start circuitry(PWM means 910, see Fig. 8) for generating the first and second start signals in response to a regulated voltage across the common load, a reference voltage, and the first and second ON-time pulses. Smith further discloses a first stop circuitry(first control means 970, see Fig. 8) for generating the first stop signal in response to the first regulator input voltage and the reference voltage, and a second stop circuitry(second control means 999, see Fig. 8) for generating the second stop signal in response to a first output current from the first converter output voltage supplied to the common load, a second output current from the second converter output voltage supplied to the common load, and the first ON-time pulse.

However Smith fails to disclose the system being a computer system also comprising one or more central processing units (CPUs), a memory for storing

instructions and data for the CPUs, and a power system for supplying power to the computer system.

Nakagawa teaches a computer system(personal computer, see column 1, lines 23-24) also comprising one or more central processing units (CPUs)(MPU, see column 1, line 15), a memory for storing instructions and data for the CPUs, and a power system(power supply apparatus, see column 1, line 23) for supplying power to the computer system. Though memory is not specifically included in referenced invention memory is inherent within the computer system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Smith and Nakagawa in order to establish a multiphase buck converter system for a computer environment. The motivation to do so would be supply appropriate voltage for the central processing unit in a computer system.

As to claim 18, Smith discloses the system wherein the first stop circuitry comprises a capacitor(capacitor 956, see Fig. 11A) charged by a current from the first regulator input voltage when the first ON-time pulse has the first logic state and discharged when the first ON- time pulse has the second logic state, and first compare circuitry(controller 90, see Fig. 11A) for comparing the reference voltage to a capacitor voltage across the capacitor and generating the first stop signal, wherein the first stop signal has a first logic state when the capacitor voltage is greater than the reference voltage and a second logic state when the capacitor voltage is less than the reference voltage.

As to claim 19, Smith discloses the system wherein the second stop circuitry comprises peak circuitry for generating a peak voltage(output voltage of the error amplifier, see column 49, line 22) proportional to a peak value(threshold level, see column 49, line 43) of the first output current. Smith also discloses first sense circuitry for generating a first sense voltage(V sub FB, see Fig. 11A) proportional to the second output current, and second compare circuitry(controller 960, see Fig. 11A) for comparing the first sense voltage to the peak voltage and generating the second stop signal, wherein the second stop signal has a first logic state when the first sense voltage is greater than the peak voltage and a second logic state when the first sense voltage is less than the peak voltage.

As to claim 20, Smith discloses the system wherein the first sense circuitry comprises a first sense resistor(resistors 941 and 942, see Fig. 11A) having a first terminal coupled to the first converter output voltage and a second terminal coupled to the common load, and a differential amplifier(error amplifier, see column 48, line 39) having a positive input coupled to the first terminal of the first sense resistor and a negative input coupled to the second terminal of the first sense resistor, and an output generating the first sense voltage.

As to claim 21, Smith discloses the system wherein the peak circuitry comprises a second sense resistor(resistors 941 and 942, see Fig. 11A) having a first terminal coupled to the second converter output voltage and a second terminal coupled to the common load. Smith also discloses a differential amplifier(error amplifier, see column 48, line 39) having a positive input coupled to the first terminal of the second sense

resistor and a negative input coupled to the second terminal of the second sense resistor, and an output generating the second sense voltage, and a sampling circuit(flip-flop 930, see Fig. 11A) for tracking the second sense voltage when the first ON- time pulse has the first logic state and holding a value of the second sense voltage as the peak voltage when the ON-time pulse has the second logic state.

As to claim 22, Smith discloses the system wherein the start circuitry comprises a compare circuit(controllers 950 and 960, see Fig. 11A) for comparing the regulated voltage across the common load to the reference voltage and generating a gate signal having a first logic state when the reference voltage is greater than the regulated voltage and a second logic state when the reference voltage is less than the regulated voltage. Smith also discloses a first select circuit(controller 950, see Fig. 11A) for generating the first start signal in response to the first ON-time pulse, the gate signal, the second start signal, and an initialization signal, and a second select circuit(controller 960, see Fig. 11A) for generating the second start signal in response to the second ON-time pulse, the gate signal, the first start signal, and the initialization signal.

As to claim 23, Smith discloses the system wherein the sampling circuit comprises a capacitor(capacitors 979 and 989, see Fig. 11B) having a first terminal coupled to ground and a second terminal, and an electronic switch(first control means 970, see Fig. 11B) for coupling the second sense voltage to the first terminal of the capacitor when the first ON-time pulse has the first logic state, the capacitor holding the value of the sense voltage as the peak voltage when the first ON-time pulse has the second logic state.

As to claim 24, Smith discloses the system wherein the first select circuit comprises a compare logic circuit(controllers 950 and 960, see Fig. 11A) for generating a compare logic signal in response to the regulated voltage across the common load, the reference voltage, and the initialization signal, and an initialization pulse(R/C clock, see Fig. 11A) circuit for generating an initialization pulse in response to the initialization signal and the compare logic signal. Smith also discloses a first logic circuit(controller 950, see Fig. 11A) for generating the first start signal in response to the first ON-time pulse, the initialization pulse, and the second start signal, and a second logic circuit(controller 960, see Fig. 11A) for generating the second start signal in response to the second ON-time pulse, the initialization pulse, and the first start signal.

As to claim 25, Smith discloses the system wherein the compare logic circuit comprises a comparator(controllers 950 and 960, see Fig. 11A) for comparing the reference voltage to the regulated voltage across the common load and generating a compare output signal having a first logic state when the reference voltage is greater than the regulated voltage across the common load and a second logic state when the regulated voltage across the common load is greater than the reference voltage, and a logic gate(controllers 950 and 960, see Fig. 11A) generating the compare logic signal as logic combination of the compare output signal and the initialization signal.

As to claim 26, Smith discloses the system wherein the initialization pulse circuit comprises a logic gate(rectifier 988, see Fig. 11B) generating a start converter signal as a logic combination of the initialization signal and the compare logic signal, and a pulse

circuit(second control means 999, see Fig. 11B) generating the initialization pulse in response to a logic transition of the start converter signal.

As to claim 27, Smith discloses the system wherein the first logic circuit comprises a flip-flop(flip-flop 930, see Fig. 11A) having an output(Q), an inverted output(Q/), a data input(D), a set input(D), a reset input(D), and a clock input(CK), wherein the set input is coupled to the initialization pulse, the clock input is coupled to the second start signal, and the inverted output is coupled to the data input. Smith also discloses a positive pulse circuit(second control means 999, see Fig. 11B) having an input coupled to the first start signal and an output coupled to the reset input of the flip-flop and generating a reset pulse in response to a logic transition of the first start signal, and an inverted pulse circuit(inverted buffer amplifier 982, see Fig. 11B) having an input coupled to the first ON-time pulse and an output generating an inverted pulse, wherein the inverted pulse circuit generates the inverted pulse in response to a logic transition of the first ON-time pulse. Smith further discloses a third logic circuit(rectifier 988, see Fig. 11B) having a first input coupled to the compare logic signal, a second input, a third input coupled to the output of the inverted pulse circuit, and generating the first start signal, and a delay circuit(dual clock generator 920, see Fig. 11A) having an input coupled to the output of the flip-flop and a delay output coupled to the second input of the third logic circuit, wherein the delay circuit selectively delays a logic transition of the delay output.

As to claim 28, Smith discloses the system wherein the second logic circuit comprises a positive pulse circuit(second control means 999, see Fig. 11B) having an

input coupled to the second start signal and an output generating a reset pulse on a logic transition of the second start signal, and a logic gate(rectifier 933, see Fig. 11A) having a first input coupled to the initialization pulse, a second input coupled to the output of the positive pulse circuit, and an output generating a gated reset pulse as a logic combination of the initialization pulse and the output of the positive pulse circuit. Smith also discloses a flip-flop(flip-flop 930, see Fig. 11A) having an output(Q), an inverted output(Q/), a data input(D), a reset input(D), and a clock input(CK), wherein the reset input is coupled to the output of the logic gate, the clock input is coupled to the first start signal, and the inverted output is coupled to the data input, and an inverted pulse circuit(inverted buffer amplifier 982, see Fig. 11B) having an input coupled to the first ON-time pulse and an output generating an inverted pulse, wherein the inverted pulse circuit generates the inverted pulse in response to a logic transition of the first ON-time pulse. Smith further discloses a third logic circuit(rectifier 988, see Fig. 11B) having a first input coupled to the compare logic signal, a second input, a third input coupled to the output of the inverted pulse circuit, and generating the second start signal, and a delay circuit(dual clock generator 920, see Fig. 11A) having an input coupled to the output of the flip-flop and a delay output coupled to the second input of the third logic circuit, wherein the delay circuit delays a logic transition of the delay output.

As to claim 29, Smith discloses the system wherein the differential amplifier is a transconductance amplifier for converting a voltage across the first sense resistor to a

first sense current coupled to a first resistor thereby generating the first sense voltage across the first resistor(see column 48, lines 36-60).

As to claim 30, Smith discloses the system wherein the differential amplifier is a transconductance amplifier for converting a voltage across the second sense resistor to a second sense current coupled to a second resistor thereby generating the second sense voltage across the second resistor(see column 48, lines 36-60).

As to claim 31, Smith discloses the system wherein the first ON-time pulse is generated as an output of a latch set by a first logic state of the first start signal and reset by a first logic state of the first stop signal(see Fig. 11A and 11B).

As to claim 32, Smith discloses the system wherein the second ON-time pulse is generated as an output of a latch set by a first logic state of the second start signal and reset by a first logic state of the second stop signal(see Fig. 11A and 11B).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

Michael J. Brown
Art Unit 2116

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100